The Application of Hardware in the Loop for Single Phase Converters Based on DSP Controller at Solar Energy Systems

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***Abstract*—The purpose of this paper is to build an effective Hardware-in-the-Loop (HIL) simulation platform for developing and testing DSP-controlled power converters. The HIL is a form of real-time simulation and differs from conventional simulations. The real-time requirements for such simulations depend on the time-scale of the process and the simulated components involved. A high-performance real-time simulation environment is necessary to obtain high precision results when time steps are too small. In this study, the detailed implementation of a very-low-cost real-time HIL simulation using open-source operating system and a relatively advanced hardware platform using averaged switch approach for the embedded controllers is presented. The proposed system consists of PC-based open-source Real Time Operation System (RTOS) and DSP. The sample rate of this system is reduced to 15 µs range based on RTOS. As an example, the HIL testing approach is applied for the controller design of AC-DC Power Factor Correction (PFC) converter. The consistency of the experimental results with the theoretical results proves the applicability of the proposed testing approach. This approach will be useful for power electronics application of solar systems.**

***Index Terms*—hardware in the loop, real time, DSP, power converter, power factor correction, renewable energy**

I. Introduction

In recent years, the use of advanced power electronics systems and their complexity increases. As a consequence, comprehensive simulation tools are needed to reduce the time to market, the complexity and costs of projects.

Traditionally, non-real simulation tools such as Simulink, Pspice and Labview are used in the development and problem-solving for power electronics studies. They have two major drawbacks: first, the computer model doesn't run at the same rate as the actual modeled system in classical simulation tools. This means that the amount of real time required to compute response of modeled system is much greater than duration of accelerated simulation time step. Second, the simulated process can't be operated with the real control hardware.

For these reasons, Real Time Digital Simulation (RTDS) is needed. Hardware-in-the-Loop (HIL) simulation is a kind of real-time simulation that allows a modeled system to interact with real hardware components. General structure of the HIL simulation is shown in Fig. 1. This simulation methodology allows testing a part of system under different real operating loads and conditions.

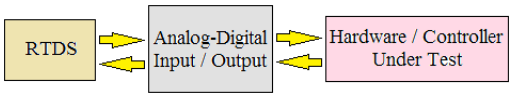

Figure 1. Hardware in the loop simulation.

The HIL simulation has been largely used in a broad range of applications such as aerospace [1]-[3], automotive [4]-[6], industrial [7], renewable energy sources [8]-[10], transmission line [11] and robotics systems [12].

This paper focuses on the power electronics applications. Currently, the HIL simulation has become widely used for designing and testing controllers under normal and abnormal operating conditions in the power electronics applications. The controller tested in hardware is presented in [13]-[19].

A real time simulator of Field-Programmable Gate Array (FPGA) for power electronics and drive systems is presented in [13], for an induction machine and permanent synchronous motor drive using FPGA is reported in [14], [15]. These systems is just soft real-time. FPGA-based control of an induction motor drive is presented in [16]. Although the FPGA-based real-time digital simulator has the small time step, a lack of library in Hardware Description Language (VHDL) as the modeling language used in power electronics applications increases development time.

A Digital controller and application for power converters are implemented in [17], [18] to design and test control systems. Although the HIL simulation for power electronics controls is implemented in [19] using open-source software, it hasn't the small time step.

It is possible to establish the HIL simulators with suitable high speed I/O ports. However, due to the hardware limitation a conventional HIL simulator has a relative long simulation step-size, which means limits its application in DC-DC converters with higher switching frequency. The important requirement of the real-time simulation is to ensure that the computation for a time-step is accomplished within the chosen step-size.

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In this study, the converter is modeled via the averaged switch approach as an alternative control method because the modeled system's equations can be solved fast enough within the chosen small time size.

Only the controller (which is executed in the external DSP controller) is tested in HIL simulation). Power electronics part (which runs in a Personal Computer (PC)) is simulated in the real-time. This method can be called "Controller HIL simulation (CHIL)". CHIL simulation has every often been employed in power electronics applications for the assessment of the controller boards. This approach allows the design and test of DSP-controlled power converters.

The contents of this paper are organized as follows; the proposed framework is described in Section II. For validation purposes, power factor correction converter is presented in Section III. The Section IV demonstrates in detail how the system works. The simulation and experimental results are given in Section V and VI respectively. Finally, the conclusion is presented in the last section.

II. The Proposed Framework

The RTDS platform is a computer having a dual-core Intel processor running at 3GHz with 8GB RAM. An open-source Real Time Operating System (RTOS) called QNX Neutrino 6.2.0 is used to achieve an efficient performance. An interrupt-driven framework developed is configurable and maximum sustainable interrupt frequency is 9 microseconds. Besides, the HIL is performed by using a PCI-E I/O board is placed in the computer to provide external interface capability. The controller is executed in the external DSP controller. The Block diagram of the proposed framework is pictorially depicted in Fig. 2.

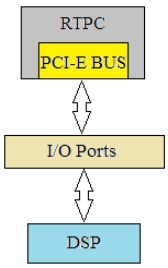

Figure 2. The block diagram of the proposed framework.

III. The Analiysis of Power Factor Correction Converter

There are different topologies used in PFC converters. The topology used in this study, is an AC-DC PFC converter and is shown in Fig. 3 [20]-[24]. An important advantage of this topology over the similar PFC converters is that the conduction losses of the semiconductor switches are lower [25]. This is due to minimum number of semiconductor switches in the current path at any instant of operation which is two [26]. This topology is composed of two single-phase boost converters without input rectifier as used in other PFC circuits [27], [28].

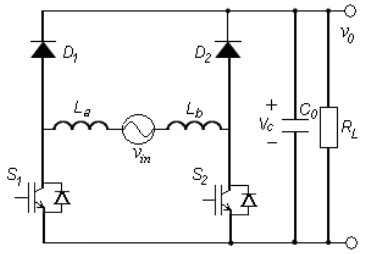

Figure 3. AC-DC PFC converter topology.

The output voltage regulation and the current control are achieved by controlling the switch S_1 during positive and S_2 during negative half cycles of the ac input voltage. The different operating modes of the converter in CCM during positive and negative half cycle of input voltage are shown in Fig. 4(a) and Fig. 4(b), respectively.

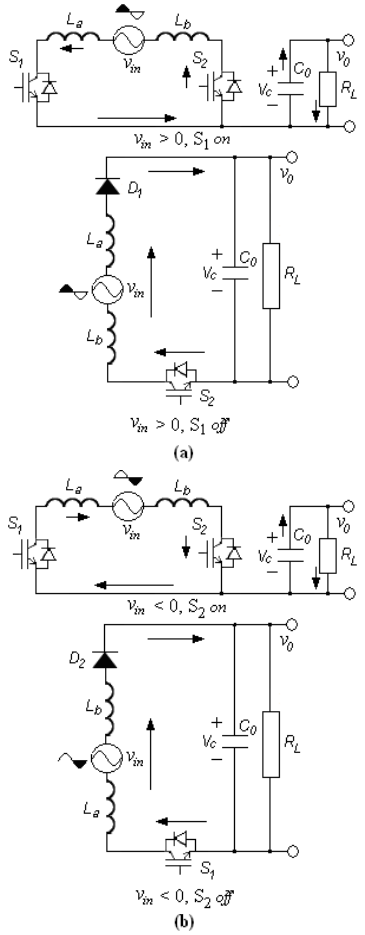

Figure 4. Equivalent circuits of the converter for on/off states of the switches during: (a) positive half cycle, (b) negative half cycle.

The mathematical model of the converter during positive half cycle of ac input voltage is given in (1) and (2). During the on state of the switch S_1 the current flows through switch S_1 and the body diode of S_2. During this period, energy is stored in the inductors and the capacitor discharges through the load ($0<t<dT_s$).

$$v_{in} = L\frac{di_L}{dt} \tag{1}$$

$$C_0\frac{dV_0}{dt} = -\frac{V_0}{R_L} \tag{2}$$

During off state of switch S_1, the current flows through D_1, the parallel connected capacitor and load and the body diode of S_2 ($dT_s<t<T_s$).

$$v_{in} - V_0 = L\frac{di_L}{dt} \tag{3}$$

$$C_0\frac{dV_0}{dt} = i_L - \frac{V_0}{R_L} \tag{4}$$

The equations corresponding to negative half cycle of ac input voltage are the same as those for positive half cycle (Equations (1)-(4)). The models corresponding to time intervals of $0<t<dT_s$ and $dT_s<t<T_s$ are given in (5) and (6), respectively.

$$\begin{bmatrix}\frac{d|i_L|}{dt}\\ \frac{dV_0}{dt}\end{bmatrix} = \begin{bmatrix}0 & 0\\ 0 & -\frac{1}{R_L C_0}\end{bmatrix}\begin{bmatrix}|i_L|\\ V_0\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}|v_{in}| \tag{5}$$

$$\begin{bmatrix}\frac{d|i_L|}{dt}\\ \frac{dV_0}{dt}\end{bmatrix} = \begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C_0} & -\frac{1}{R_L C_0}\end{bmatrix}\begin{bmatrix}|i_L|\\ V_0\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix}|v_{in}| \tag{6}$$

The average voltage across the inductor and the average capacitor current is zero in steady state. State-space averaged switch approach for this converter in the case of Continuous Conductive Mode (CCM) is given in (7).

$$\begin{bmatrix}\frac{d|i_L|}{dt}\\ \frac{dV_0}{dt}\end{bmatrix} = \begin{bmatrix}0 & -\frac{1-d}{L}\\ \frac{1-d}{C_0} & -\frac{1}{R_L C_0}\end{bmatrix}\begin{bmatrix}|i_L|\\ V_0\end{bmatrix} + \begin{bmatrix}\frac{d}{L}\\ 0\end{bmatrix}|v_{in}| \tag{7}$$

where Ts, $L=L_a+L_b$, $d=T_{on}/T_s$, C_0, and R_L are the switching period, input inductance, duty cycle ration, output capacitance and load, respectively.

The differential equations cannot be solved analytically; however, in science and engineering, a numeric approximation to the solution is often good enough to solve a problem. The implicit trapezoidal integral rule is implemented for discretization and formulating the converter equations that has the following general form:

$$x(n+1) = x(n) + \frac{h}{2}[f(x(n+1)) + f(x(n))] \tag{8}$$

where h is the step time. Applying the implicit trapezoidal rule for the inductor and the capacitor in (7), we have:

$$I_L(n+1) = I_L(n) + \frac{h}{2L}[2v_{in} - (1-d)(V_0(n+1) + V_0(n))] \tag{9}$$

$$V_0(n+1) = V_0(n) + \frac{h}{2C}[(1-d)(I_L(n+1) + I_L(n)) - \frac{1}{R_L}(V_0(n+1) + V_0(n))] \tag{10}$$

Equation (10) is rearranged and the output voltage equation of converter is given by:

$$V_0(n+1) = \frac{1}{a_1}[V_0(n) + a_2(I_L(n+1) + I_L(n)) - a_3 V_0(n)] \tag{11}$$

where:

$$a_1 = 1 + \frac{h}{2CR_L}, a_2 = (1-d)\frac{h}{2C}, a_3 = \frac{h}{2CR_L} \tag{12}$$

The input current of the converter can be obtained by inserting (11) in (9):

$$I_L(n+1) = \frac{1}{1+a_6}[(1-a_6)I_L(n) + (a_7 - a_5 - a_8)V_0(n) + a_4 v_{in}] \tag{13}$$

where:

$$a_4 = \frac{h}{L}, a_5 = \frac{(1-d)h}{2La_1}, a_6 = \frac{(1-d)ha_2}{2La_1}$$
$$a_7 = \frac{(1-d)ha_3}{2La_1}, a_8 = \frac{(1-d)h}{2L} \tag{14}$$

The block diagram of the controller is shown in Fig. 5. There are two loops in the program. The inner loop is responsible for controlling the shape of the input current and the outer loop controls the output voltage and keeps it constant at the reference value. Outer loop employs a PI controller to perform its task. In outer loop, the output voltage level is scaled and compared with the reference value to obtain error which makes the input of the PI controller [29]. Output of this particular controller is the scaling factor and is used to obtain the current reference. In inner loop, the rectified input current is compared with reference current and the result is processed to be used to generate average duty cycle ratio.

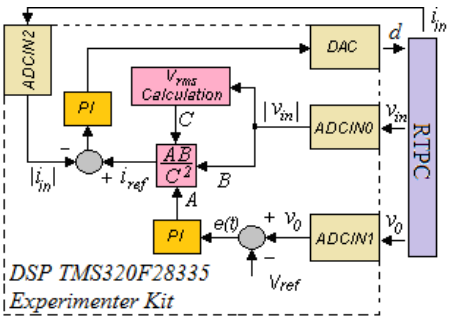

Figure 5. Proposed controller block diagram.

IV. The Controller Application on Proposed Framework

In order to succeed PFC through the HIL, the TMS320F28335 eZdsp experimenter kit was chosen for the embedded control system of PFC. The hardware interface to the computer is an Advantech PCLD-8712, low-cost DAQ card inserted into PCI-E slot of the computer. Configuration of the HIL system is shown in Fig. 6. The interface consists of Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs). It is assumed that the ADCs are an ideal sampler with a sampling period.

The CHIL simulation is to test the control algorithm in the controller. The controller inputs are the inductor current, the input and the output voltages. The controller output is the averaged duty cycle ratio. The computer interacts with the eZdsp board through the I/O board attached to PCI-E slot of its. By using this board the

software running on the computer can read the averaged duty cycle ratio data and exports the inductor current, the input and output voltages data to the eZdsp in each interrupt for one sample interval. The eZdsp board receives 3 analog signals such as the inductor current, the input and the output voltages from the computer. These signals are converted from analog to digital through the ADCs when the controller receives these signals from the modeled power converter system; it executes the control algorithm for one sample interval. The controller returns the averaged duty cycle ratio computed during this step to the computer through the PCI-E slot. At this point, one sample cycle of the RT simulation is completed and the modeled power converter system proceeds to the next sample interval. The process repeats and the simulation progresses.

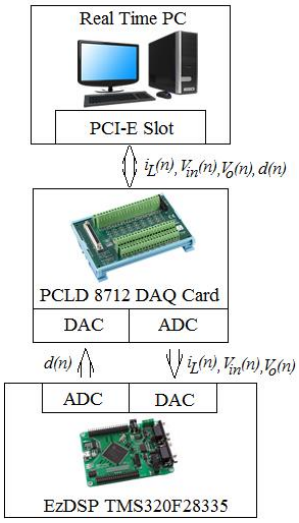

Figure 6. Configuration of the HIL system.

V. The Study of Simulink Simulation

The parameters used in simulations and experiments are given in Table I. First, simulation studies are performed in MATLAB/Simulink tool by using these parameters and the results are given in Fig. 7 and Fig. 8.

TABLE I. Parameters Used in Simulations and Experiments

Output Power	P_o	500 [W]
Output voltage	V_o	400 [V]
Input voltage	v_{in}, f_{line}	220 [V_{rms}, 50 Hz]
Switching frequency	f_s	50 [kHz]
Step time	h	15 µs
Inductance value	L_a	1.5 [mH]
Inductance value	L_b	1.5 [mH]
Output Capacitor	C_0	470 [µF]

Fig. 7 shows the inductor current and output voltage response of the converter for full load (P_o=500W) and the load setting is changed from 500W to 250W after reaching the steady, then again up to 500W in Fig. 8.

Although the simulation run time for this operation is 0.5s, the elapsed time in order to finish this execution is around 15s. For longer time simulations, the time required for developing and testing the embedded controller can be important.

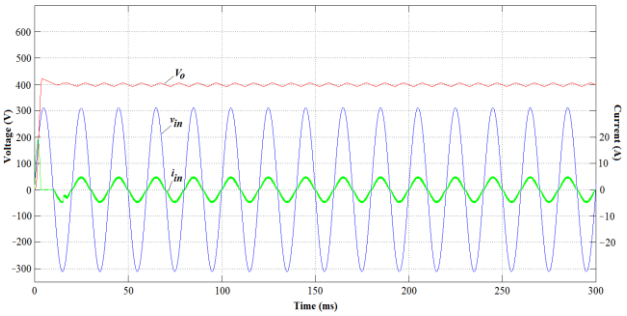

Figure 7. From top to down output voltage (V_o), input voltage (v_{in}) and inductor current (i_L) of the closed-loop system.

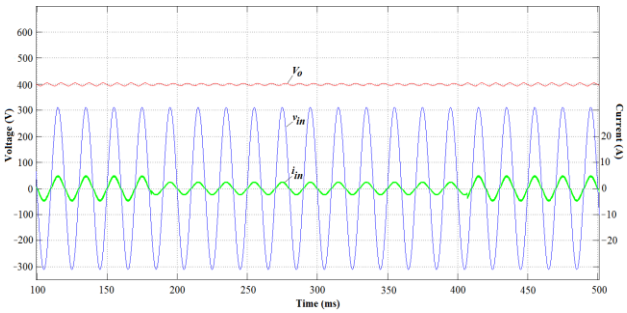

Figure 8. From top to down output voltage (V_o), input voltage (v_{in}) and inductor current (i_L) of the closed-loop system with change in load settings.

VI. The Study of Hardware in the Loop Simulation

The schematic diagram of the controller is given in Fig. 5. The real-time library contains all the elements needed for the simulation. These elements include the converter model and the embedded controller using averaged switching as alternative control method. One thread was used to implement the main loop of the timer interrupt subroutine. This thread was run at the highest priority permitted by the RTOS. The total time needed to execute the time step iteration was 15 µs. The Implicit trapezoidal integration method was used for the HIL simulation. By using this system 0.5 second simulation execution took only 0.55 seconds.

All the calculated data is stored on the dynamic memory by allocating circular buffers during runtime. And just after simulation ends these data are copied from the dynamic memory to the file system. The purpose of storing data in memory during runtime is not to access to hard drive and by this way reduce the sampling interval since accessing the dynamic memory is faster than accessing to hard drive. The data processed during runtime is written in the files just after the execution ends and the data written in the hard drive are formatted so that it can be plotted.

Fig. 9 and Fig. 10 show the waveforms obtained on the HIL simulation. It is obvious that general behaviors as well as instantaneous responses are very similar.

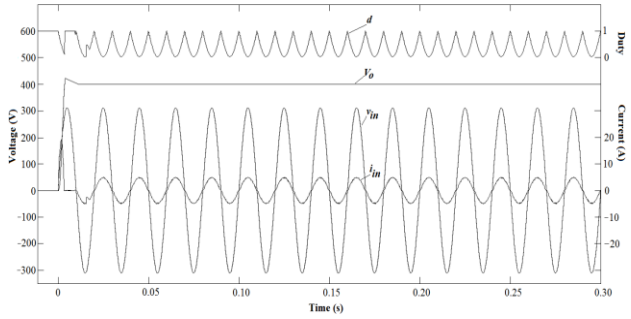

Figure 9. From top to down duty cycle ratio (d), output voltage (V_o), input voltage (v_{in}) and inductor current (i_L) of the closed-loop system in the HIL Simulation.

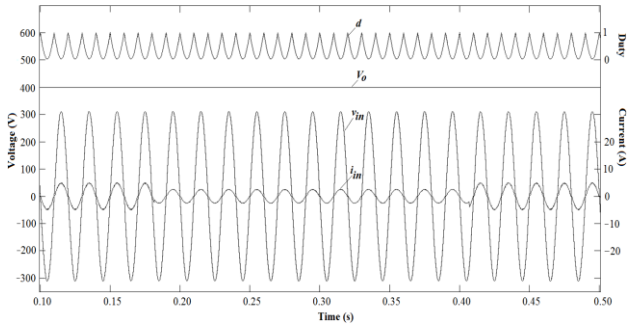

Figure 10. From top to down: duty cycle ratio (d), output voltage (V_o), input voltage (v_{in}) and inductor current (i_L) of the closed-loop system with change in load settings in the HIL simulation.

The algorithm is adapted to Matlab program that is given as follows:

```
L=0.001;
C=0.0005;
RL=40;
vm=311;
w=2*pi*50;
d=0.2;
h=0.000015;
ILold=0;
Vo=0;
a1=1+h/(2*RL*C);
a2=h*(1-d)/(2*C);
a3=h/(2*RL*C);
a4=h/L;
a5=h*(1-d)/(2*a1*L);
a6=h*(1-d)*a2/(2*L*a1);
a7=h*(1-d)*a3/(2*L*a1);
a8=h*(1-d)/(2*L);
        for i=1:100000
           array_IL(i+1)=ILold;
        ILnew=((1-a6)*ILold+(a7-a5-
        a8)*Vo+a4*abs(vm*sin(w*i*h)))/(1+a6);
        if ILnew<0
        ILnew=0;
        end
array_Vo(i+1)=Vo;
array_vin(i+1)=abs(vm*sin(w*i*h));
Vo=(Vo+a2*(ILnew+ILold)-a3*Vo)/a1;
ILold=ILnew;
end
```

VII. Conclusion

This paper describes a low-cost HIL simulation platform for developing and testing DSP-controlled power converters. The hardware and software used in the HIL simulation are suitable for an educational laboratory. The HIL simulation has been compared and validated with Simulink simulation. The simulation results demonstrate the effectiveness of the proposed simulation technique. This simulation infrastructure can be developed by adding new mathematical models and improving the sampling time, so this system can be used for detailed analysis of more complex systems. By this way, test duration of verification-validation can be decreased for complex systems. This proposed system will be useful for renewable energy sources.

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