Low Power Testing of VLSI Circuits Using Test Vector Reordering

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***Abstract*—Power consumption is one of the biggest challenges in high performance VLSI design and testing. Low power VLSI circuits dissipate more power during testing when compared with that of normal operation. Dynamic power has been the dominant part of power dissipation in CMOS circuits, however, in future technologies the static portion of power dissipation will outreach the dynamic portion. The proposed approach is based on a reordering of test vectors in the test sequence to minimize the average and peak power of the circuit using test application. In this paper weighted switching activity is derived based on the average power consumed in the logic gates during all possible event conditions. Since this weighted switching activity is based on the power, the proposed method gives more accurate results. The proposed algorithm is implemented and verified using ISCAS85 benchmark circuits. Power is estimated for the circuits using Tanner EDA tool. The results show that power is reduced significantly over the existing methods.**

***Index Terms*—weighted switching activity, test power, reordering, power dissipation, power matrix**

I. Introduction

Power consumption has recently become a serious consideration in IC design and testing. Maximizing circuit speed and minimizing chip area used to be the only major concerns of VLSI designers. The growing size of VLSI circuits, high transistor density, and popularity of low power circuit and system design are making minimization of power dissipation an important issue in VLSI design. In recent years, power consumption of integrated circuits (ICs) has been proved to be just as important of a concern. Thus, VLSI designs nowadays emerge as a tradeoff among three goals: minimum area, maximum speed, and minimum power dissipation [1]. Excessive power dissipation causes overheating, which may lead to soft errors or permanent damage. It also limits battery life in portable equipment. Thus, there is a need to accurately estimate the power dissipation of an IC during the design phase.

A lot of low power design techniques have been proposed at all levels of the design hierarchy. In test mode, the switching activity of all nodes often is several times higher than the activity during normal operation. Since heat or power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test can cause several problems.

Excessive switching activity due to low correlation between consecutive test vectors can cause several problems. First, since heat dissipation in a CMOS circuit is proportional to switching activity, the circuit can be permanently damaged when the circuit experiences more switching activity [2], [3] during its operation. Second, it has been observed that metal migration or electro-migration causes the erosion of conductors and subsequent failure of circuits [2], [4]. Since temperature and current density are major factors that determine electro-migration rate, elevated temperature and current density caused by excessive switching activity during test application can severely influence the reliability of CUT. In this paper, test vector reordering method is proposed to minimize the testing power more effectively. Weighting factors derived from power dissipation due to two successive test vectors are considered while reordering the test vectors.

II. Existing Methods

Many research works have tried to solve the power problem in high performance VLSI circuits. Test vector ordering with vector repetition has been presented as a method to reduce the average as well as the peak power dissipation of a circuit during testing. It also reduces the total switching activity by lowering the transition density at the circuit inputs. Experimental results validate that the proposed technique achieve considerable savings in energy and average power dissipation while reducing the length of the resulting test sequences compared to the original method. Based on re-ordering of the test-pair sequences, the switching activities of the circuit-under-test during test application can be minimized. Hamming distance between test-pair is defined to guide test-pair re-ordering. It minimizes power dissipation during test application without reducing delay fault coverage [5].

The reordered test vector set with minimum hamming distance is used for testing the CUT to reduce the switching power. Hamming Distance approach is based on the concept that the internal switching activity is more or less depending on the hamming distance at the input of the circuit. This concept is not true for all the circuits and the switching activity is depending on the logic gates that

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are used to construct the circuit. In the work by Chakravarty and Dabholkar [6], the authors construct a complete directed graph in which each edge represents the number of transitions activated in circuit after application of the vector pair. The authors use a greedy algorithm to find a Hamiltonian path of minimum cost in the graph.

A scheme [7] is proposed by Chattopadhyay and Choudhary for reducing the hamming distance between consecutive patterns in the test set using a genetic algorithm based approach. As the hamming distance reduces, the switching activity in the circuit is also expected to reduce. Also Girard *et al.* [2] propose using the Hamming distance between test vectors rather than the number of transitions in the circuit to evaluate the switching activity produced in the CUT by a given input test pair. Using the Hamming distance makes it possible to apply test vector reordering to large VLSI designs. Hamming distance method may not be accurate all the times, the bit change at the input of the circuit may or may not reduce the switching activity of the circuit. Reducing the hamming distance will not assure the power optimization. To overcome the difficulty, the actual switching activity is considered for reordering the test vectors. Other reordering algorithms based on hamming distance [8] and internal switching activity [9]-[11] also found in literatures.

III. Back Ground and Related Work

A. Energy and Power Modeling

Power dissipation is an important issue in both the design and test of VLSI circuits. Power consumption in CMOS circuits can be classified as static and dynamic. Static power dissipation is due to leakage current or other current drawn continuously from the power supply which contributes very slightly in the overall power dissipation.

The total leakage current in logic gates includes two components, namely, sub threshold and gate leakage. Dynamic power consists of switching power and short circuit power. Short circuit current flows during the time when both transistors are in ON state. It depends on the rise or fall times of the input waveform. It also depends on the load output capacitance. Decreases for larger output load capacitance. The peak short circuit current occurs at the time when the transistor switching off goes from linear to saturation region. Switching power results from the activity of a circuit in changing its states due to the charging and discharging of the effective capacitive loads. Dynamic power significantly contributes to total power dissipation.

Three parameters are important for evaluating the power properties of a CUT during testing. The consumed energy directly corresponds to the switching activity generated in the circuit during test application, and has impact on the battery lifetime during remote testing.

The average power consumption is given by the ratio between the energy and the test time. This parameter is even more important than the energy as hot spots and reliability problems may be caused by constantly high power consumption.

The peak power consumption corresponds to the highest switching activity generated in the CUT during one clock cycle. If the peak power exceeds certain limits, the correct functioning of the circuit is no longer guaranteed. For CMOS circuits, dynamic power is the dominant source of power consumption which is consumed when nodes switch from 0 to 1 or from 1 to 0.

The energy consumed at node i per switching is

$$½C_iV^2_{DD} \quad (1)$$

where C_i is the equivalent output capacitance and V^2_{DD} is the power supply voltage [12]. Hence, a good approximation of the energy consumed in a period is $½C_iS_iV^2_{DD}$ where S_i is the number of switching during the period. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, and in a first approximation, capacitance C_i is assumed to be proportional to the fan-out of the node F_i [13].

Static dissipation is due to leakage current and this current is usually neglected during estimation. Hence, dynamic power dissipation is dominant. Dynamic power dissipation occurs at a node when it switches from one logic level to other level. Dynamic power dissipation divided into two components caused by charging and discharging current and short circuit current. The static power dissipation is caused when both pMOS and nMOS transistor are simultaneously ON during small interval of switching period, the current flows directly from the power supply to ground and this current is negligible for high speed circuits. Short circuit current is caused by the switching activity of transistors during 0 1 or from 1 0 transitions. The charging and discharging of the circuit, the capacitor charges and discharges the output of the gate during 0 1 or from 1 0 transitions. The dynamic power dissipation of the circuit is given by

$$1/2C_L(l)S(l)V^2_{DD} \quad (2)$$

where

$C_L(l)$ is the load capacitance of the Circuit Under Test (CUT),

$S(l)$ is the frequency of switching of the line V_{DD} is the power supply voltage.

To reduce the switching activity the simplest way is the test vector re ordering. This modified test vector sequence is applied to CUT, heat dissipation is minimized. Weighted switching activity based re ordering method is introduced to approximate the power with more accuracy. This method is more accurate than other techniques. Nodes connected to more than one gate are nodes with higher parasitic capacitance. Based on this fact, capacitance C_L is proportional to the fanout of the node. Therefore, an estimation of the consumed energy E_i at node i is

$$E_i=½.S_i.F_i.C_o.V^2_{DD} \quad (3)$$

where C_o is the minimum output load capacitance. According to this expression, the estimation of the energy consumption at the logic level requires the calculation of the fan-out F_i and the number of switching on node i, S_i.

The total WSA in the circuit during application of the complete test sequence is

$$WSA=\Sigma\,\Sigma\, S(i,k)*Fi \quad (4)$$

IV. Proposed Method

The power dissipation during testing [3] is minimized by reducing the number of transitions in the circuit. Usually test vectors are in random and hence it is necessary to rearrange the order of occurrence of test vectors so that minimum switching activity between successive test vectors is obtained. In this proposed method weighting factors are evaluated using average power dissipation during every gate transitions.

The existing methods used hamming distance, switching activity and weighted switching activity based on fan-outs for reordering of test vectors. In weighted switching activity method each and every gate transitions are estimated to get approximate power. Though event occurs, depends up on the logic of the circuit switching activity may or may not be occurred in the particular gate. Hence, mere switching activity will not approximate the dynamic power precisely. Hence, power based weighting factor will give more precise solution for reordering of test vector. Also it includes static and dynamic power. But the drawback is the time complexity to evaluate power for all possible pair of test vectors. So in order to overcome the time complexity problem and to approximate the power accurately, the weighting factor based on average power will give better solution.

In this proposed method, average power for all possible initial and final conditions are evaluated for all logic gates such as AND, OR, NAND, NOR, XOR, XNOR, NOT are determined by implementing in Tanner EDA tool. Initial inputs to basic gates such as AND as A=0, B=0 are considered. When there is a transition from 0 0 to 1 0, the output is 0 for which average power consumed is determined as 89 µW. While transition of inputs from 0 0 to 0 1, the output is same as 0 and the average power consumed for this transition is 342 µW. Observing the above two conditions, it is understood that average power produced is with large difference though the output and number of transitions are same. Hence weighting factors are calculated based on the average power consumed for all possible transitions of input. Average power includes both static and dynamic power.

Test vectors are reordered based on these weighting factors [14] for minimizing test power in combinational circuits.

Weighting factor can be calculated by using the following formula.

$$\text{Weighting factor for transition} = \frac{\text{Average power during transition}}{\text{Minimum average power}} \quad (5)$$

For example, transition in NAND gate 1 1 to 1 0, consumes 963 µW and the weighting factor is 963/45=24 while 45 µW is minimum average power for the transition 00 to 11. All the possible transitions and their weighting factor for NAND gate are given in Table I.

The problem of minimizing switching power is solved by graph theory using Hamiltonian path [11] technique. Graph G (V, E) is defined with V nodes and E edges. The problem is formulated by considering the test vector as node and weighting factors between them as edge cost of the graph. The graph considered here is complete graph whose all the nodes are connected each other with edges. Adjacency matrix for the graph is represented by average power weighting factor matrix APWF [ ] [ ] of order n x n.

The matrix element APWF [i][j] represents weighting factor based on average power in the CUT when j^{th} test vector is applied after i^{th} test vector. In this graph, the Hamiltonian path is a path connected by all nodes with minimum total edge cost. Reordering algorithm is used to construct the Hamiltonian path, which is resultant reordered test vector set with minimum average power in CUT [11]. Hence this path offers reduced power dissipation in the CUT during testing [5]

TABLE I. Weighting Factor for NAND Gate

Transitions at Inputs A,B		Output	Average Power	Weighting Factor
From	To			
0 0	0 1	1	315 µW	8
0 1	0 0	1	293 µW	7
0 0	1 0	1	84 µW	2
0 1	1 0	1	580 µW	15
0 1	1 1	0	45 µW	1
1 0	0 0	1	345 µW	9
1 0	0 1	1	127 µW	3
1 1	0 1	1	554 µW	14
1 0	1 1	0	57 µW	1
1 1	1 0	1	963 µW	24
0 0	1 1	0	45 µW	1
1 1	0 0	1	920 µW	23

Heuristic approach is used in the algorithm to find more suboptimal sequences. The more suboptimal solutions can be obtained when two or more values of APWF matrix APWF [ ] [ ] are identical. These solutions are called heuristic based sub-optimal solutions. The reordering algorithm used to minimize the average power during testing is given as follows

A. Reordering Algorithm

The various parameters used in the algorithms are as follows:

$t_1, t_2, \ldots t_n$ be n test vectors with m bits each.

T={1, 2, … k … n} where k represents k^{th} position in the vector set generated by ATPG. R is a set to store ordered test vector sequence.

Q is a set to store {T-R}.

Step1: Select an element APWF [x_{min}] [y_{min}] in the power matrix such that which is smallest value in the matrix. Add x_{min}, y_{min} to R; Q←{T-R}; x←y_{min}.

Step2: Select a test vector y_{min} such that APWF [x] [y_{min}] is minimum in the array.

Step3: Add y_{min} to R; Q←{T-R}; x←y_{min}.

Step4: Repeat the above two steps till Q becomes empty.

This algorithm is applied to reorder the test vectors in ISCAS85combinational benchmark circuits

B. Results and Discussions

The simple ISCAS85 [15] benchmark circuit C17 and complex C432 circuit is modeled to show the effectiveness of the proposed algorithm. The test set consists of 6 vectors for C17 as shown in Table II and 36 vectors and are serially numbered for C432 respectively. The C17 and C432 circuits are modeled in CMOS ML_0.25 (Technology) using T spice simulator of Tanner pro EDA tool and average power is calculated for reordered set.

TABLE II. DETAILS OF BENCHMARK CIRCUITS

Circuit	No of gates	Inputs	Outputs	No of test vectors	Fault coverage
C17	6	5	2	6	100%

Each circuit is implemented using VHDL to calculate the Average Power Weighting Factor matrix (APWF). APWF matrix for C17 benchmark circuit is

$$APWF=\begin{pmatrix} 0 & 35 & 58 & 42 & 36 & 74 \\ 68 & 0 & 91 & 22 & 78 & 95 \\ 41 & 70 & 0 & 60 & 57 & 27 \\ 79 & 23 & 54 & 0 & 78 & 93 \\ 57 & 43 & 57 & 80 & 0 & 36 \\ 54 & 67 & 34 & 83 & 51 & 0 \end{pmatrix} \quad (6)$$

The waveform for evaluation of APWF Matrix in C17 Circuit is shown in Fig. 1. By using the wave form APWF matrix is derived and the above APWF matrix is used in the reordering algorithm and the sub optimal solutions are generated. This matrix is obtained by evaluating the average power of CUT after applying any two test vectors of unordered test set successively. The matrix is used for the reordering test vectors with the help of the algorithm.

More number of reordered test sets generated by using different test vectors as seed value as shown in TABLE III.

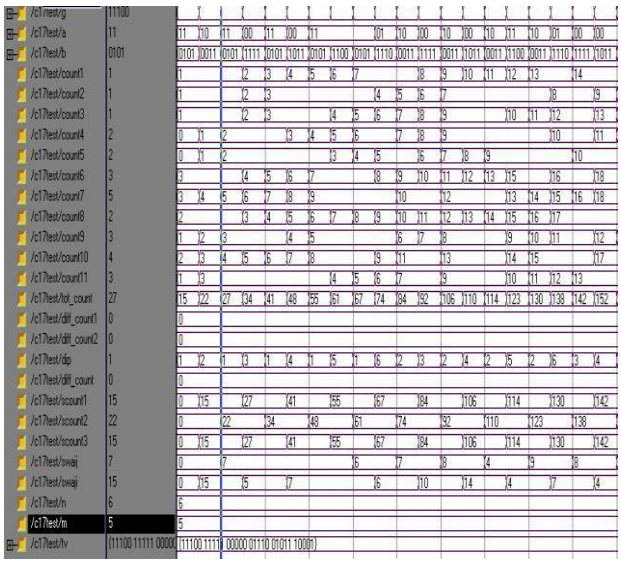

Figure 1. Waveform for evaluation of APWF matrix in C17 circuit

TABLE III. REORDERED TEST VECTOR SET

Unordered	Seed 1	Seed 2
11100	10001	11011
11111	00011	01011
00000	10010	00011
01110	10110	10001
01011	01011	10010
10001	11011	10110

All the sets are used to evaluate both average power and peak power. The results are tabulated in Table IV and Table V for average power and peak power respectively. The results are also compared with unordered test sets and switching activity based reordered test set [9]-[11].

It shows that the average power is reduced upto 12.4% for switching activity based method and 59% for proposed method for circuit C432. Similarly peak power is reduced upto 99% for the proposed method. The circuit C17 does not show any difference in reorder power because it is a smaller circuit with very minimum number of test vectors and hence it has no other better reordered sequence to reduce its power

TABLE IV. REORDERED AVERAGE POWER FOR BENCHMARK CIRCUITS

Ckt	Unordered	Reordered Average power			
		Switching activity		Weighting factor Based	
		reordered	%improved	reordered	%improved
C17	6.127mW	4.244mW	30.73%	4.244mW	30.73%
C432	144.85mW	126.8mW	12.4%	59.38mW	59%

TABLE V. REORDERED PEAK POWER FOR BENCHMARK CIRCUITS

Ckt	Unordered	Reordered Peak power			
		Switching activity		Weighting factor Based	
		reordered	%improved	reordered	%improved
C17	65.69mW	38.82mW	40.90%	38.82mW	40.90%
C432	27.03mW	565.02mW	97.9%	87.03mW	99%

Above results shows that weighting factor based reordering algorithm gives better results when compared with existing methods. Since both Static and Dynamic power are included in the proposed method, it is more suitable for latest VLSI Circuits where Static power is increased with higher proportion with Dynamic power.

V. CONCLUSION

In VLSI design process, power dissipation during testing is major concern. In this project a novel method is proposed for test power minimization to get accurate results. Since the total power dissipation is higher due to switching activity, the proposed algorithm is to reduce the switching activity by reordering the test vectors by considering the weighting factor evaluated based on average power in the logic gates. This method is implemented in ISCAS85 benchmark circuits using tanner pro EDA tool to evaluate the average and peak power. Results show that an improvement is achieved for average and peak power with unordered test set and existing method

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