A Leakage Current Induced by Barrier Metal Formation in Power MOSFETs with Trench Contact Structure

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***Abstract*—One of important parameter of Power MOSFET is ON resistance (RON) to minimize power loss in power system. To minimize RON, need high cell density process because channel resistance has occupied high proportional for total RON in low voltage Power MOSFET. Trench contact structure is suitable for high density device with narrow contact width. However in this structure case, designer should consider silicide formation due to high aspect ratio profile to prevent high leakage current. In this paper, present optimized Ti/TiN thickness formation to minimize leakage current between Drain and Source. Basically it shows good leakage performance that all removed Ti/TiN layer on the top of ILD by additional etchback or CMP process. And another finding from our study, optimized Ti/TiN formation also shows comparable leakage current with it. Unreacted Ti(+) ion is main contributed factor for high leakage current at P-channel device and higher wafer stress due to thicker TiN layer is another factor.**

***Index Terms*—trench gate power MOSFET, trench contact structure, on resistance, leakage current, silicide**

I. Introduction

The major design considerations of a trench gate power MOSFET are lowering of ON resistance (RON), enhancement of Drain breakdown voltage, reduction in switching delays, enhancement in dV/dt capability, high damage immunity while switching large current in inductive loads and minimization of energy losses. In terms of energy efficiency is concerned, there are two types of energy losses in a power MOSFET that need to be suppressed. The first and foremost is the conduction loss arising from the non-zero RON and the other one is the switching loss caused by charging and discharging of the gate electrode while switching the device ON and OFF. This charge is known as gate charge (QG) [1]. The major efforts made for reducing RON are usually based on the lateral and vertical scaling or pitch reduction. This approach is effective in reducing the channel resistance. To meet the requirement of low RON, a very high channel density is necessary that can be achieved by scaling down the trench and contact width using DUV lithography and the self aligned fabrication process because otherwise the alignment tolerances between two lithography steps may become a bottleneck. One of a way to implement of high density device has commonly used trench contact structure with silicidation and filled in metal plug such as tungsten. Titanium silicides are currently used in MOS technology. However, in the conventional way of forming the silicide that is by deposition of a titanium layer and further annealing, the required for the reaction silicon is consumed from the substrate. Trench contact structure device has something different silicide formation since source metal contacted to cover two different current paths one is sidewall of trench contact at on state current flow and others trench contact bottom area to current flow at off state as shown Fig. 1. Hence designer should consider minimum contact resistance and leakage current induced by both areas. In this paper we present an optimized barrier metal formation for minimum Drain-Source leakage current in trench contact Power MOSFET device.

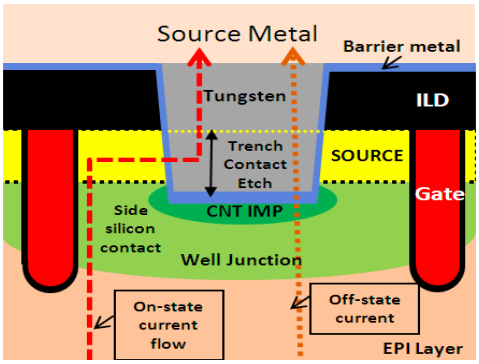

Figure 1. Schematic vertical cross section of Power MOSFET with trench contact structure and major current flow line.

II. Device Structure and Silicide Process

Most of important requirement of Power MOSFET is lower RON to minimize power loss in the power system. RON is decided depends on resistance of current path between Drain with Source and high proportional factor is density of channel number in lower voltage Power MOSFET. Trench contact structure can be kept source contact width regardless of the cell pitch because the source contact is formed at the sidewall of the trench. Thus more effective than surface contact structure for

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reducing the RON by reducing the cell pitch as shown Fig. 1. Power MOSFET has a parasitic bipolar transistor which causes a destructive breakdown when it is activated by, for example, unclamped inductive load switching (UIS) [2]. To enhance UIS performance, have to reduce Base resistance at Well junction. Trench contact structure can be reduced it because can makes minimum off state current path as trench contact Etch depth control.

The important point of scaling down the structure to high cell density is the minimize contact width with low contact resistance. TiSi2 is a popular silicide because it has the lowest resistivity of all silicides. Silicide formation is normally consists of Titanium (Ti) deposition to formed TiSi2 layer, Titanium nitride (TiN) deposition for barrier metal and then rapid thermal anneal (RTA). Titanium nitride is an attractive material as a contact diffusion barrier in silicon manufacturing, because it behaves as an impermeable barrier to silicon and because the activation energy for the diffusion of other impurities is high. TiN is also chemically and thermodynamically very stable. The TiN specific contact resistivity to silicon is somewhat higher than that of Ti or PtSi, and as result, it is ordinary not used to make direct contact to Si. Instead it, contact structure consisting of TiN-Ti-Si or TiN-TiSi2-Si was most commonly been used. Such contact structures exhibit very low specific contact resistivity to Si and remarkably high thermal stability, with the ability to withstand temperatures up to 550 ◦C without contact failure [3]. In the case of W-plug technologies, TiN barrier failure can lead to current leakage or the volcano problem, due to the reaction of fluorine ions with Ti atoms under the TiN barrier film. Tungsten hexafluoride (WF6) is used during the W-plug deposition process. The TiN film acts as a barrier between the ions from and the Ti-wetting layer under the TiN [4].

III. Experimental

The main steps for the fabrication of Power MOSFET with trench contact structure are described as follow. N-type and P-type epitaxial wafers (100) were taken the starting material and Trench Gate silicon was etched by DPS etch using LPTEOS hard mask. To make smooth silicon surface and corner round formed sacrificial oxidation with high temperature and all removed by HF wet etchant. The gate oxide was thermally grown. In case of N-channel device, doped N-type Poly-Si layer was deposited to fill the trench gate but, P-channel device case, deposited un-doped Poly-Si and then doping via high dosage Implant process. And Poly CMP carried out to planarization. Dopant ions were implanted and diffused for formed Well junction and source junction. ILD deposited by APCVD. The contact trenches, which penetrated the source region and reached to the Well junction region, were formed by DPS tool. Dopant ions were implanted to bottom of trench contact and annealed. Ti/TiN deposited range from 500A to 1000A. Tungsten deposited by CVD to fill the contact trenches. Thick aluminum was deposited and defied to make the electrodes for source and gate.

IV. Result and Discussion

A. Titanium (Ti) Effect to Leakage Current.

Basically designer can select two ways for remain Ti/TiN layer on top of ILD in the Power MOSFET device. One is still remain this layer and another way is all etch away by additional etch tool. As per with or without Ti/TiN layer etch, leakage current performance is quite different as shown Fig. 2. In case of remain Ti/TiN layer, leakage current is higher from low voltage reverse bias condition and almost two order higher than all removed condition at -30V reverse bias condition. But this result shows only P-channel device. The reverse leakage current of N-channel device is not shows significant different between with or without Ti/TiN etch.

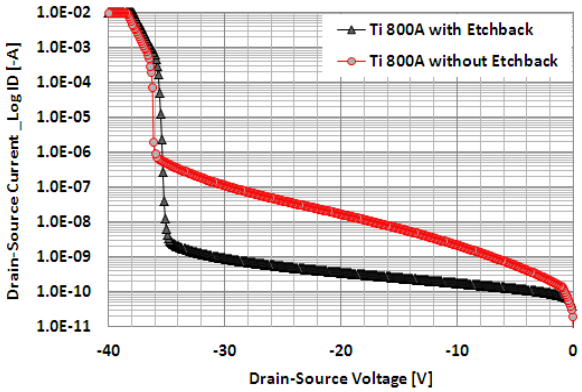
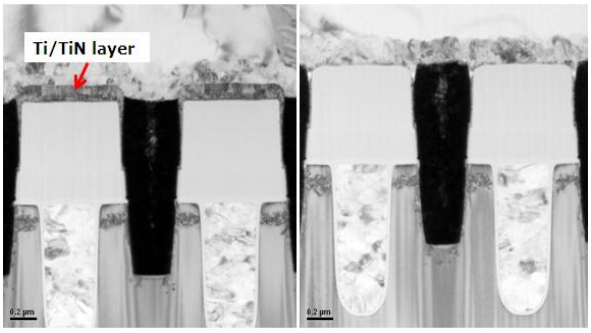


Figure 2. VD-ID graph regarding the Ti/TiN etchback effect for P-channel -30V device.

The main active cell structures for different Ti/TiN layer formation on top of ILD are shown Fig. 3.



(a) (b)

Figure 3. TEM cross sectional picture for (a) remain Ti/TiN layer on top of ILD (b) all removed Ti/TiN layer.

Reverse bias leakage current and RON performance between Drain and Source for various Ti thickness are shown Fig. 4. Even though still remain Ti/TiN layer on top of ILD, leakage current shows lower at below Ti thickness 500Å condition. And in terms of RON parameter is also related with Ti thickness. At below Ti thickness 500Å condition, Ron is slightly higher but comparable with Ti/TiN removed condition which means even Ti thickness reduce until 300A it could be not much increased contact resistance. But, RON@VGS=4.5V parameter quite higher at Ti thickness 800Å condition, it

could be related with threshold voltage. The channel resistance (Rch) is given by

$$Rch = \frac{L}{Z\,\mu ns\;Cox\,(VG-VT)} \quad (1)$$

where Z and L are the width and length of the channel and μns is the surface mobility of electrons. The channel resistance will be lower when threshold voltage (VT) is higher given by equation (1). This VT effect to channel resistance is strong in case of lower VGS RON test parameter. That is why RON@VGS=4.5V parameter drift is higher than RON@VGS=10V parameter.

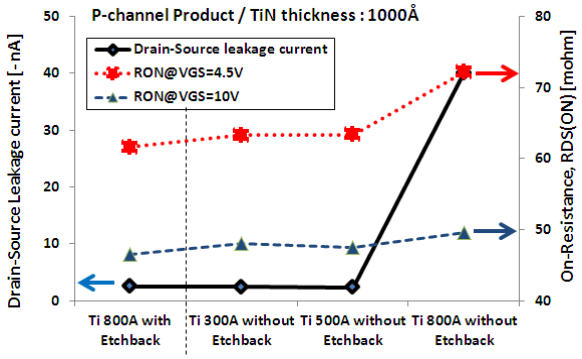
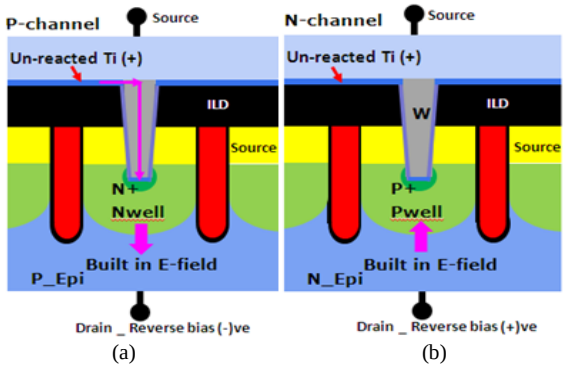


Figure 4. Drain-source leakage current and ON resistance for various Ti thickness and with or without Ti/TiN etchback

We would like to postulate that the increase leakage current in P-channel Ti 800Å without etch back condition is related to a built-in electric field between P_Epi and Nwell junction in early reverse bias period after that, as reverse bias higher, leakage current dramatically increase induced by unreacted Ti(+) ion that placed on top of ILD as shown Fig. 5(a). As shown in Fig. 5(b) for N-channel device, this built-in electric field points towards the source area for N-Epi / Pwell junction which means unreacted Ti(+) ion can't diffuse to Drain node at a state of equilibrium and reverse bias condition as well because Drain biasing should positive (+ve) at N-channel reverse bias condition. In this paper, we would like to propose that Ti diffusion enhanced by a built-in electric field Nwell/P-Epi junction can cause an increase in leakage current of a Nwell/P-Epi junction with a enough thickness of unreacted Ti(+) ion.



(a) (b)

Figure 5. The direction of built in electrical field in (a) N-channel device (b) P-channel device, illustrating for leakage current increase only P-channel device due to un-reacted Ti (+) ion.

For the threshold voltage comparison with various Ti thickness, as Ti thickness increase, N-channel and P-channel device shows oppsite trend at without etchback condition as shown Fig. 6. Even though remain Ti/TiN condition, threshold voltage is the same as all remove Ti/TiN condition at Ti thickness 300Å. P-channel deive threshold voltage is increased but, N-channel device is decreased at thicker Ti condition. This symtom also could be explaned with unreacted Ti(+) ion effect.

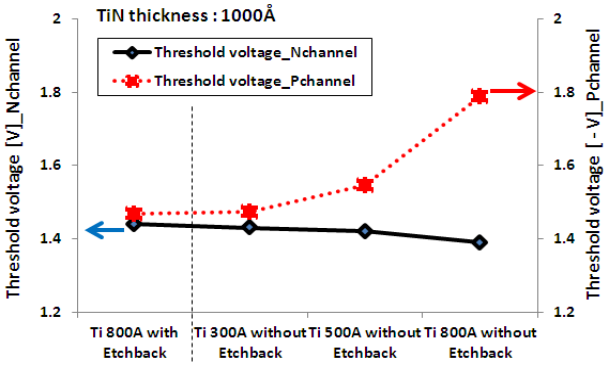
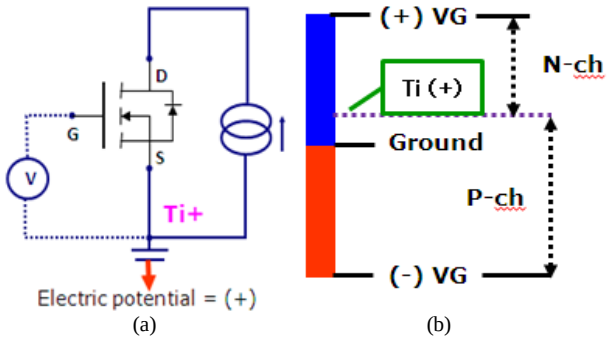


Figure 6. Threshold voltage for various Ti thickness and with or without Ti/TiN etchback

Threshold voltage is given by,

$$V_T = \varphi_{ms} + \frac{Qs}{Cox} + 2\varphi_B - \left(\frac{Qss+Q_I+Q_{FC}}{Cox}\right) \quad (2)$$

where, Q_{ms} is difference of metal and the semiconductor work function and Qs is surface charge, φ_B is buck potential. Qss is interface chage, Q_I is mobile charge, Q_{FC} is fixed surface change. In actual MOS structure, the threshold voltage is altered due to several factors. One is unequal work function for the metal and the semiconductor. And all of gate oxide charges cause a shift in the theshold voltage [5]. Unreacted Ti(+) ion which placed on top of ILD and connected source electrod, it could not change to difference of metal and the semiconductor work function (φ_{ms}) and gate oxide related charges. But electric potential point of view, source is not zero ground. As shown Fig. 7(b) because source has positive potential, theshold voltage of N-channel could be lower and P-channel theshold voltage is drifted toward higher.



(a) (b)

Figure 7. (a) Equivalent circuit for Threshold voltage test. (b) Electrical potential between Gate and Source.

B. The Effect of Titanium Nitride (TiN)

TiN layer has been widely used as barrier metal in silicon fabrication field. Based on our study, thicker TiN film can be increased leakage current due to higher wafer stress as shown Fig. 8. As per this probability chart of leakage failure site is increased as TiN thickness higher within the whole wafer. And this failure rate is increased in direct proportion with active die size it means that wafer yield is lower at bigger die size device. It could be explained with film stress related. A Ti film has tensile stress as deposited. However, oxide and TiN films are compressive stress as deposited. Due to the tensile film between the two compressive films, the overall stress value before the RTA step yields low compressive stress. After the RTA step, the TiN film exhibits a high tensile stress due to grain growth, together with the Ti under layer film causing an increase in the overall tensile stress values [6]. When stress values higher, cracks can be generated causing a current leakage path. High tensile stress barrier films are not recommended for rough surface topographies. Thus, bottom edge of Trench structure device is quite weak against tensile stress as shown Fig. 9.

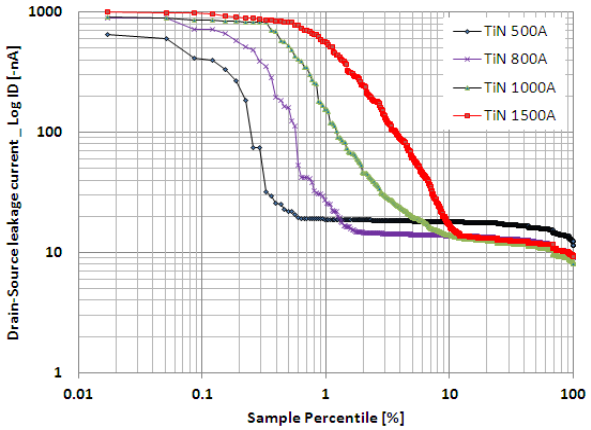


Figure 8. Probability chart of drain-source leakage current for various TiN thickness.

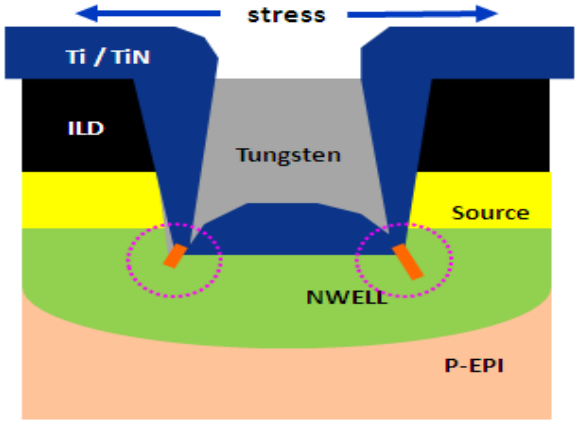


Figure 9. Zoom out cross sectional of Trench contact structure after barrier meal formation.

V. Conclusion

From the above analysis, we propose that the unreacted remain Ti/TiN formation are the major cause of high leakage current in P-channel Power MOSFET. And even though still remain Ti/TiN layer on top of ILD, leakage current could be made comparable with removed condition through optimize layer thickness respectively. Remain titanium (Ti) layer contribute not only increase leakage current but also shift threshold voltage. However, Ti thickness below 500Å condition shows comparable leakage current level and not much difference threshold voltage drift without additional etchback or CMP process. In terms of Titanium nitride effect, thicker layer shows higher leakage current due to higher wafer tensile stress. Bigger die size device shows even worse because it has lots of contact structure.

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Sian Han Chai photography and biography not available at the time of publication.

Gee Hong Tong photography and biography not available at the time of publication.