Windowed-sinc Band-pass Filter based Reference Signal Extraction for Grid Synchronization

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***Abstract*—In this paper a Windowed-sinc band-pass filter has been designed to trace the phase angle of the fundamental component of voltage at the point of common coupling (PCC). The designed filter presents very good capability in handling DC component, harmonic components, phase jump and frequency drift. It even has the capability to handle minor sub-harmonic interference. Compared with phase locked loop (PLL) based grid synchronization methods, the proposed method is easier to be implemented and full digital. Its response speed either matches or exceeds currently used synchronization methods.**

***Index Terms*—filter, grid-tie inverter, synchronization**

I. Introduction

Grid-tie inverter has been a research focus for many years. Grid synchronization is one of the fundamental issues for such connection. With ongoing booming of renewable energy, such research is gaining more momentum as it is critical to connect renewable-energy-generation-driven inverters to existing power grid [1]-[3].

The basic requirements on the methods for synchronization are 1) High immunity to the influence of DC component; 2) High immunity to the influence of harmonics; 3) high immunity to the influence of sub-harmonic components; 4) Capability to suit the phase jump during operation; 5) Capability to suit frequency change etc[4]-[6].

There are many methods that have been developed to facilitate the grid synchronization, including discrete Fourier transform, recursive discrete Fourier transform, phase locked loop (PLL) based on In-Quadrature signal generation, PLL based on Hilbert transform, and PLL based on adaptive filtering etc. Each method has its pros and cons against the above listed requirements. Some of them cannot remove the influence of sub-harmonic components while others have slow response, which could be as long as five cycles. Furthermore some of the methods are sophisticated and hard to use. These demand a new method to be developed[3]-[8].

In this paper we propose a Windowed-sinc narrow band-pass filter that can meet the above-listed requirements. In the meantime it is easier to be implemented and has fast response.

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This paper is organized as follows. In Section II, the Windowed-sinc filter is designed and its performance is examined; Section III presents Simulink implementation of the power system under study with the designed Windowed-sinc band-pass filter. Section IV concludes the paper.

II. Filter Design and its Performance

The fundamental Windowed-sinc filter kernel used in our filter design is given below by (1)

$$H(i) = K\frac{\sin\left[2\pi f_c(i - M/2)\right]}{i - M/2} \cdot\left[0.42 - 0.5\cos(2\pi i/M) + 0.08\cos(4\pi i/M)\right] \quad (1)$$

Where f_c is the cutoff frequency, expressed as a fraction of the sampling rate, a value between 0 and 0.5. The sample number kernel is determined by M, which must be an even integer. The sample number i is an integer that runs from 0 to M, resulting in M+1 total points in the filter kernel. The constant K is chosen to provide unity gain at zero frequency. To avoid a divide-by-zero error, for $i=M/2$, use $h(i)=2\pi f_c K$.

The procedure for designing a Windowed-sinc band-pass filter with a center frequency of 50Hz system is as follows:

Step 1: Design a Windowed-sinc low-pass filter with a cut-off frequency of 40Hz using (1); Normalize its kernel H1 for unity gain at DC.

Step 2: Design a Windowed-sinc low-pass filter with a cut-off frequency of 60Hz using (1); Normalize its kernel H2 for unity gain at DC.

Step 3: Change the low-pass filter in step 2 into a high-pass filter kernel H3 using spectral inversion.

Step 4: Add the normalized low-pass filter kernel H1 in Step 1 to the normalized high-pass filter kernel H3 in Step 3 to form a band-reject filter kernel H4.

Step 5: Change the band-reject filter kernel H4 in Step 4 into a band-pass filter kernel H by using spectral inversion.

The kernel of the designed band-pass filter with a center frequency of 50Hz and a band width of 40Hz through 60Hz is shown in Fig. 1.

To test the capability of the designed filter in tracing the angle of fundamental frequency component of a signal, the following signal with DC component,

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fundamental component and harmonic components are taken as shown in Eqns. (2) through (7).

$$v_1(t) = 550\sin(2\pi f_1 t + \pi/2)\,(\mathrm{V}) \quad (2)$$

$$v_3(t) = 55\sin\left[2\pi(3f_1)t + \pi/2\right](\mathrm{V}) \quad (3)$$

$$v_7(t) = 55\sin\left[2\pi(7f_1)t\right](\mathrm{V}) \quad (4)$$

$$v_{25Hz}(t) = k * 55\sin\left[2\pi(25)t\right] \quad (5)$$

$$v_{DC}(t) = 100e^{-t/0.2}\,(\mathrm{V}) \quad (6)$$

$$v(t) = v_{DC3}(t) + v_{25Hz}(t) + v_1(t) + v_3(t) + v_7(t) \quad (7)$$

The compensation angle for the filter with a center frequency of 50Hz is shown in Fig. 2, from which one can see that it is almost linear against frequency range under study.

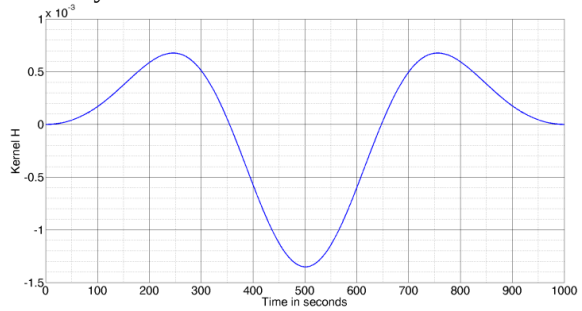

Figure 1. Kernel of designed band-pass filter with a band of 40Hz through 60Hz.

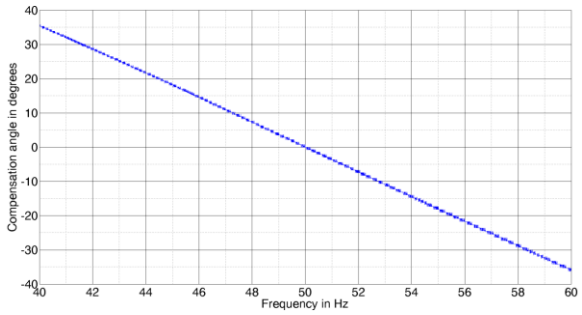

Figure 2. Compensation angle at each frequency for the designed band-pass filter with a center frequency of 50Hz.

Below are several cases with which the basic properties of the designed filter are examined.

A. *Case 1: Test of Pull-in Capability*

The signal used to check the pull-in capability of the filter is given by (8)

$$v(t) = v_{DC}(t) + v_1(t) + v_3(t) + v_7(t) \quad (8)$$

with f_1 being set to 50Hz.

The results are shown in Fig. 3 and Fig. 4, from which one can see that it takes the filter one and a half cycles to become synchronized with the fundamental component of the signal. Compared with other filters[2], it works faster.

B. *Case 2: Sudden 20% Voltage Dip in the Fundamental Component*

The used signal v(t) is $v(t) = v_{DC}(t) + v_1(t) + v_3(t) + v_7(t)$ with f_1 being set to 50Hz. The sudden 20% voltage dip happens at 0.16s. Fig. 5 shows voltage signal used for this study. Sudden voltage dip is applied to overall signals v(t). Fig. 6 shows fundamental component of total voltage and its traced fundamental by the designed filter, from which one can see that after voltage dip, the designed filter can quickly trace the change. Fig. 7 illustrates the angles, where the upper half is the angle of the fundamental of the total voltage and traced angle of the fundamental while the lower half is the angle difference between these two. From these two figures one can see that the designed filter works very well to trace the change of voltage dip and the time taken is 0.194s-0.16s or 0.034s, which is less than two cycles.

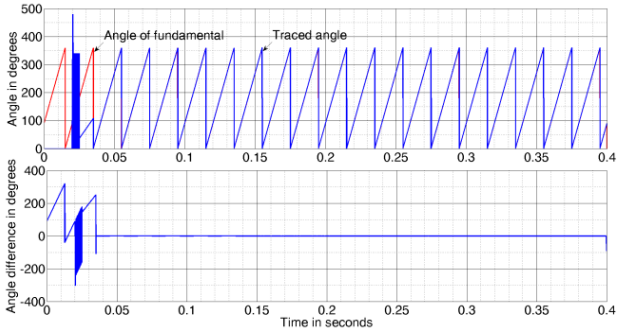

Figure 3. Pull-in performance for the designed filter with a center frequency of 50Hz.

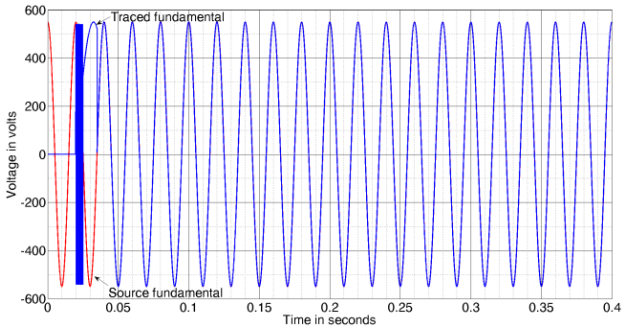

Figure 4. Fundamental component of voltage signals for examining pull-in performance for the designed filter with a fundamental frequency of 50Hz.

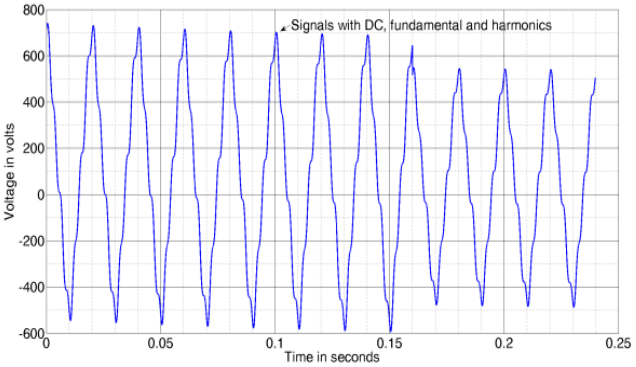

Figure 5. Signals used to study on sudden voltage dip.

C. Case 3: 600-angle Jump of Source Fundamental Component

Fig. 8 and 9 illustrate performance of the filter in the case of phase jump, from which one can see that the filter can trace new phase angle quickly. The time taken to synchronize with new phase angle of the source fundamental signal is 0.192s-0.16s=0.032s and less than two cycles.

D. Case 4: Working at 45Hz with Angle Compensation

The signal used to check this performance of the filter is given by

$$v(t) = v_{DC}(t) + v_1(t) + v_3(t) + v_7(t)$$

with f_1 being set to 45Hz.

Fig. 10 shows the traced angle when the frequency of the fundamental component is 45Hz. One can see that with the phase compensation as shown in Fig. 2 the traced angle dwell perfectly on the angle of the fundamental of the source. But the pull-in time is slightly longer than that of 50Hz as shown in Fig. 3.

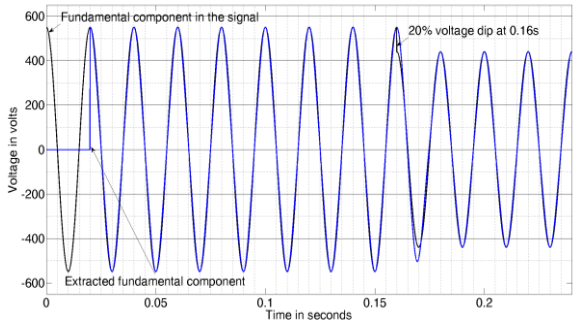

Figure 6. Fundamentals for studying sudden voltage dip.

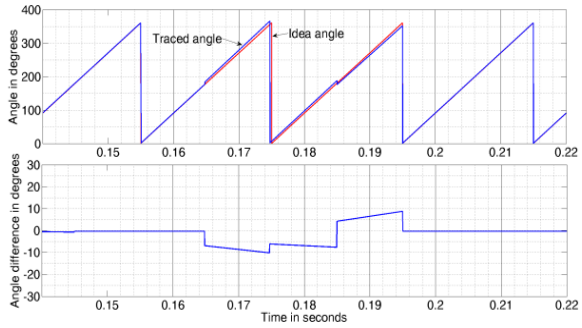

Figure 7. Angles due to a sudden voltage dip.

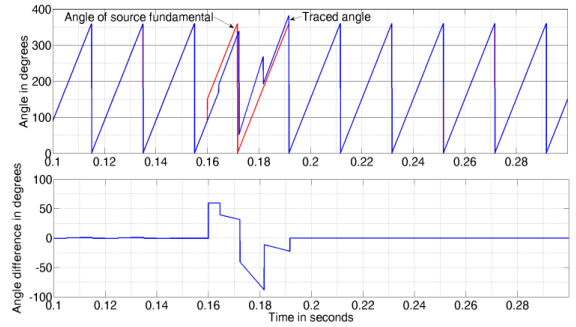

Figure 8. Angles for phase jump study.

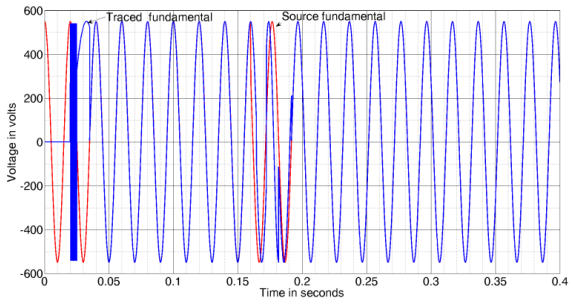

Figure 9. Fundamentals for phase jump study.

E. Case 5: Frequency Drift from 50Hz to 45Hz

Frequency jump happens at 0.16s. Fig. 11 shows angles for this case, from which one can see that the designed filter takes 0.19s-0.16s=0.03s to synchronize with the new angle of the 45Hz.

F. Case 6: Working with the Existence of Sub-harmonics

The signal used to check this performance of the filter is given by $v(t) = v_{DC3}(t) + v_{25Hz}(t) + v_1(t) + v_3(t) + v_7(t)$, with f_1 being set to 50Hz.

Fig. 12 and 13 show the performance of the designed filter with the existence of sub-harmonics of 25Hz. One can see from these two figures that the sub-harmonics have influence on the performance of the filter. When the 25Hz sub-harmonic component is 5%, the maximum phase error is 4.8^0, while when the 25Hz sub-harmonic component is 2.5%, the maximum phase error is 2.4^0.

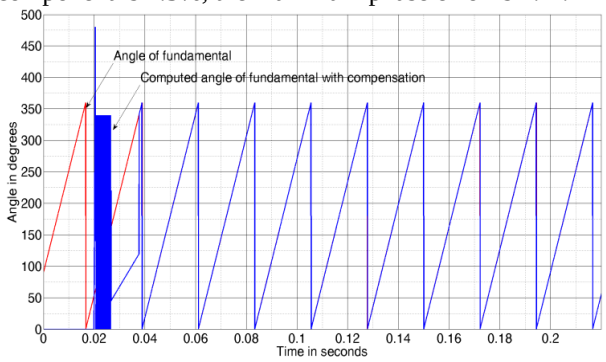

Figure 10. Traced angle when the fundamental frequency is 45Hz.

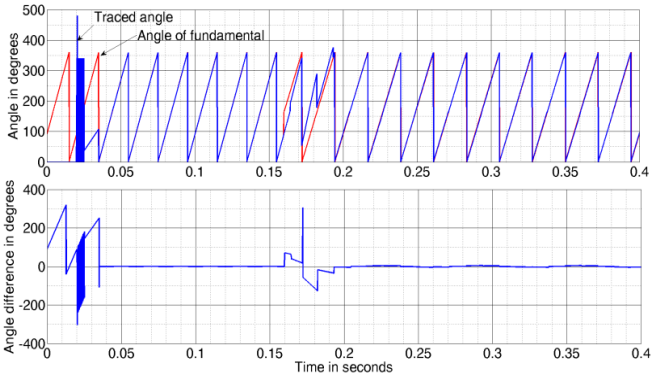

Figure 11. Angle for frequency jump of 50Hz to 45Hz.

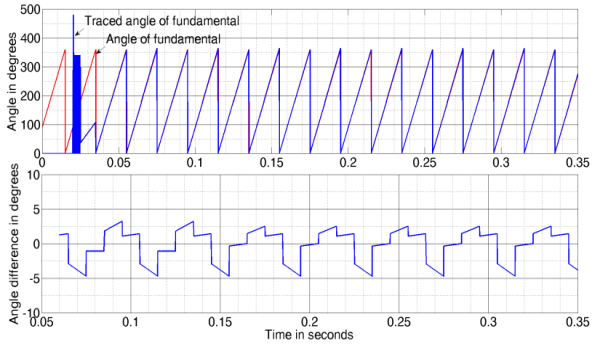

Figure 12. Angle for the performance of the filter with 5% of 25Hz sub-harmonic component.

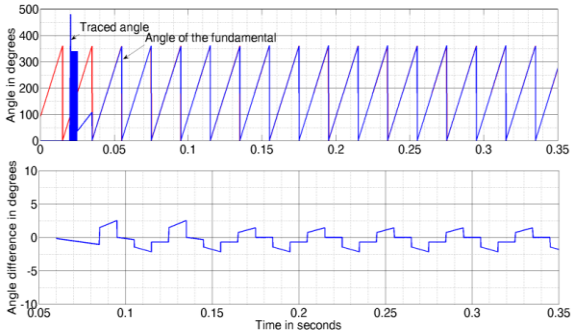

Figure 13. Angle for the performance of the filter with 2.5% of 25Hz sub-harmonic component.

III. Examination of the Designed Filter in a Power System using Simulink

To examine the performance of the designed filter in a circuit, a power system as shown in Fig. 14 is modeled in Simulink, where three-phase source voltages are

$$v_a(t) = 898\sin(2\pi 50t) \ \text{(V)} \quad (9)$$

$$v_b(t) = 898\sin(2\pi 50t - 2\pi/3) \ \text{(V)} \quad (10)$$

$$v_c(t) = 898\sin(2\pi 50t + 2\pi/3) \ \text{(V)}; \quad (11)$$

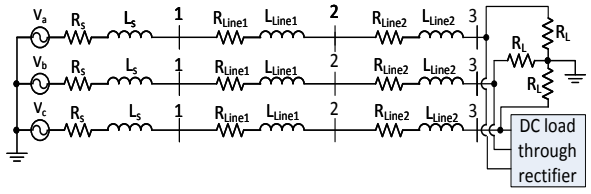

Figure 14. Circuit implement in Simulink to test the designed filter.

Source impedance information is R_s=0.1Ω, L_s=2mH; line impedance information: R_{Line1}=0.5Ω, L_{Line1}=20mH; R_{Line2}=0.5 Ω, L_{Line2}=20mH; There are two loads, one being a three-phase balanced resistive load with a resistance of R_L=80Ω in each phase and the other being a DC load powered through a naturally-commutating rectifier. The second load is switched in at 0.1s.

Point of common coupling (PCC) is chosen at bus 2. Voltage transformers at bus 2 have a voltage transformer ratio (VTR) of 50.

Fig. 15, 16 and 17 show the voltage at PCC or bus 2 and their extracted fundamentals. To examine the performance of the designed filter under more severe conditions, the DC load current is set at high value. Since it is powered through a naturally-commutating rectifier, three-phase input currents into the rectifier contain abundant harmonic components. After it is switched in, one can see that it incurs significant voltage drop across the transmission line impedance, thereby producing significant disturbance to the voltage at PCC.

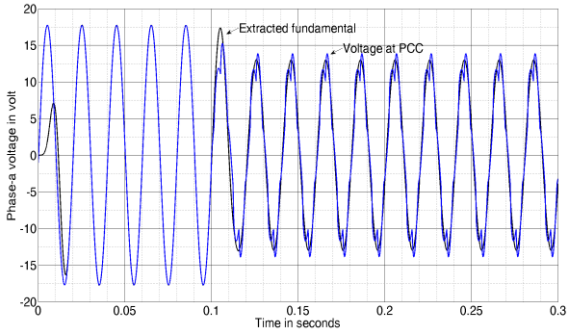

Figure 15. Phase-a voltage at PCC.

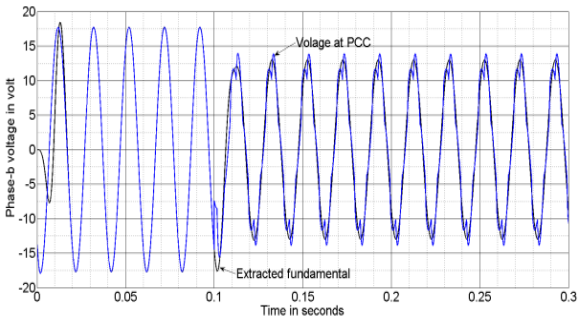

Figure 16. Phase-b voltage at PCC.

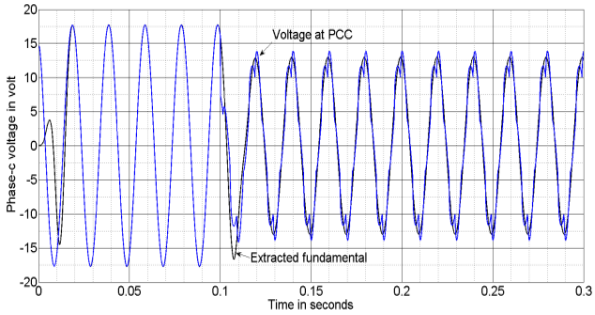

Figure 17. Phase-c voltage at PCC.

Fig. 18 shows the angle of traced fundamental component at PCC and true angle of the fundamental at PCC. The true angle of the fundamental at PCC was obtained by exporting the data of voltage at PCC to Matlab code, where its Fourier analysis was carried out and the angle of its fundamental was obtained. From Fig. 18 one can see that to pull in, the filter takes two cycles to synchronize the extracted signal with the fundamental component of the voltage at PCC. When the DC load is switched in at 0.1s, the synchronization takes around 2 cycles or 40ms.

In this paper we adopted a digital signal processor or microcontroller mimicking approach to implement the

algorithm of Windowed-sinc filter in Simulink environment instead of using z-transform or s-transform approach. Such approach is close to a real microcontroller implementation. The details are shown in the appendix.

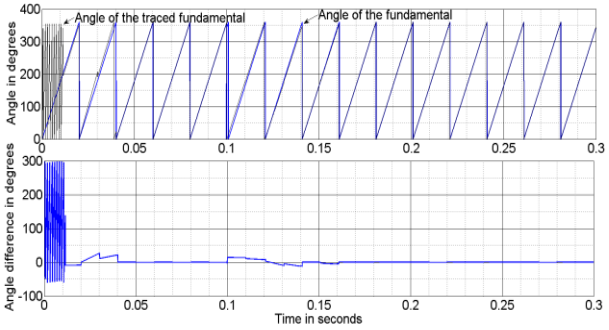

Figure 18. Phase angles and angle difference

IV. Conclusion

In this paper we proposed a Windowed-sinc band-pass filter to serve the purpose of extracting reference voltage for grid synchronization. It is found that it performs very well upon most requirements for such application. These include: 1) high immunity to the influence of DC component; 2) high immunity to harmonic components; 3) being suitable for the application of frequency drift; 4) being suitable the application of phase jump; 5) capability to remove the influence of minor sub-harmonics. Its response time matches the existing synchronization methods and it is relatively easy to use. So it is suitable for grid synchronization applications.

V. A Simulink Implementation of the Designed Filter

Fig. 19 shows the overall circuit in the Simulink for the power system given in Fig. 14. The upper half in Fig. 19 is the power system and the lower half is the block to implement the designed Windowed-sinc filter for three phases, where the input signal is the three-phase voltage from VT as shown in the upper half space. The block of "Sampling One Cycle" is data store memory and stores the number of sampling points per cycle. In our study, it is equal to 1000. This is because the sampling rate is set to 1/Ts or 1/(2E-05) or 5E04 and one cycle lasts 0.02s. Correspondingly the sampling points per cycle is 0.02*5E04=1000.

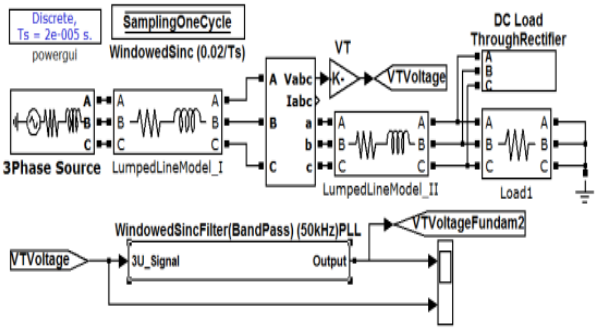

Figure 19. Overall circuit in simulink.

Fig. 20 is the block of three-phase filters. The content of "WindowedSincFilterA" in Fig. 20 is shown in Fig. 21.

In Fig. 21, several Data Store Memories are adopted which are shown at the top of the figure. There are several input signals into the block of "WindowedSincFilter" for phase-a, which include those Data Store Memories. These data are retrieved from the Data Store Memories as connected on the left side of the block and updated in the block, then output to the same Data Store Memories as connected on the right side of the block.

Part of the codes in the block of Fig. 21 is shown below. One can see that these codes are similar to C-language based digital signal processor code or microcontroller codes. They are implantable from Simulink to a real DSP or microcontroller based hardware application. Such approach shortened the distance between modeling and hardware implementation.

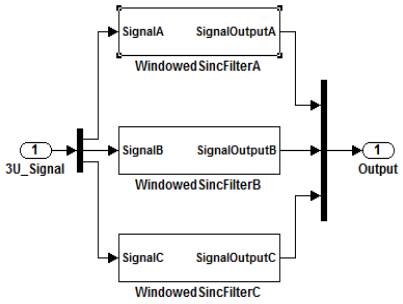

Figure 20. Three-phase filter block.

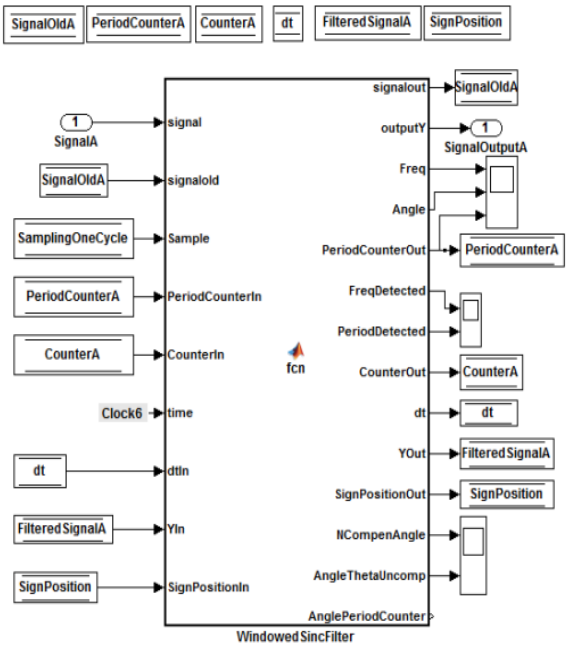

Figure 21. Block of matlab function where phase-a filter is implemented.

Example code:

```
for j1=1:Sample-1
signalold(j1)=signalold(j1+1);
end
signalold(Sample)=signal; signalout=signalold;
```

```
    Sum=0;
    for j1=1:Sample
        Sum=Sum+H(Sample-j1+1)*signalold(j1);
    end
    outputY=Sum*FundamentRatio;YOut(1)=YOut(2);
YOut(2)=outputY
     SignPosition1=SignPositionIn(1);
SignPosition2=SignPositionIn(2);
    SignY1=sign(YOut(1)*1E05);
SignY2=sign(YOut(2)*1E05);
    SignY=SignY1*SignY2;
    if SignY<0 && SignY1<0
        SignPosition1=PeriodCounterIn;
PeriodCounterIn=1;
    end
     if SignY<0 && SignY1>0
        SignPosition2=PeriodCounterIn;
    end
    SignPositionOut(1)=SignPosition1;
SignPositionOut(2)=SignPosition2;
    PeriodDetected=abs(2*(SignPosition2-
SignPosition1)*dt);
    FreqDetected=abs(1/PeriodDetected);
    CompenAngle=AngleComp(NCompenAngle);
    PeriodCounterOut=PeriodCounterIn+1;
    AngleTheta=(PeriodCounterOut*dt/PeriodDetected)*3
60-CompenAngle;
    AngleTheta=mod(AngleTheta,360);
Angle=AngleTheta*pi/180;
```

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